FIG.1

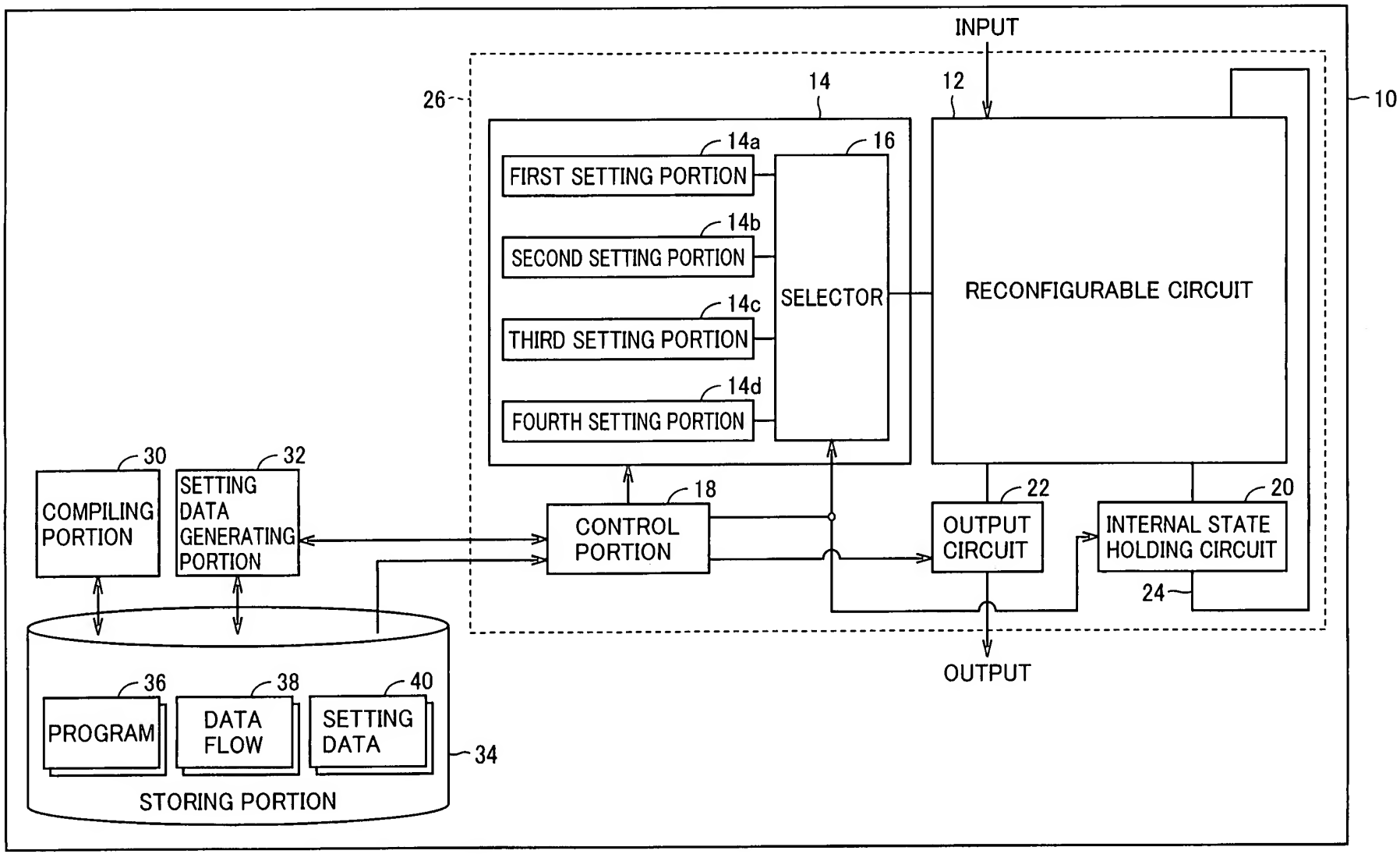

INPUT
26
14
12
10
14a
16
FIRST SETTING PORTION
14b
SECOND SETTING PORTION
SELECTOR
RECONFIGURABLE CIRCUIT
14c
THIRD SETTING PORTION
14d
FOURTH SETTING PORTION
30
32
COMPILING PORTION
SETTING DATA GENERATING PORTION
18
CONTROL PORTION
22
OUTPUT CIRCUIT
20
INTERNAL STATE HOLDING CIRCUIT
24
OUTPUT
36
38
40
PROGRAM
DATA FLOW
SETTING DATA
34
STORING PORTION

FIG.2

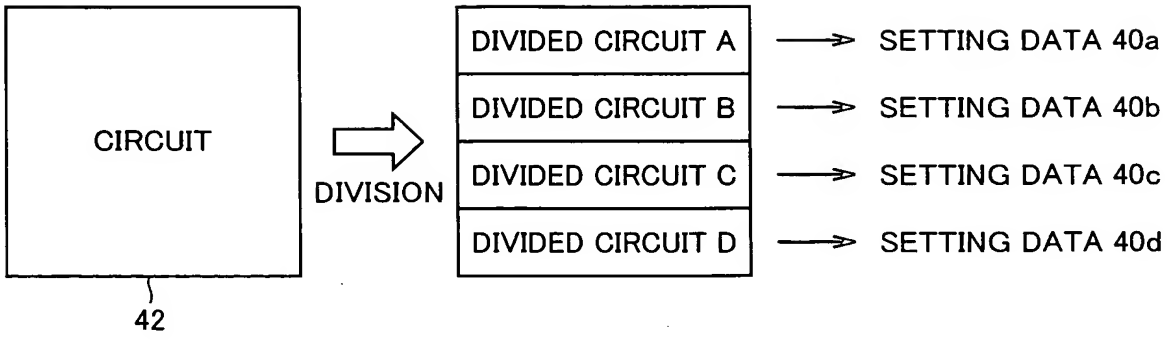

CIRCUIT
42
DIVISION
DIVIDED CIRCUIT A
DIVIDED CIRCUIT B
DIVIDED CIRCUIT C
DIVIDED CIRCUIT D
SETTING DATA 40a
SETTING DATA 40b
SETTING DATA 40c
SETTING DATA 40d

FIG.3

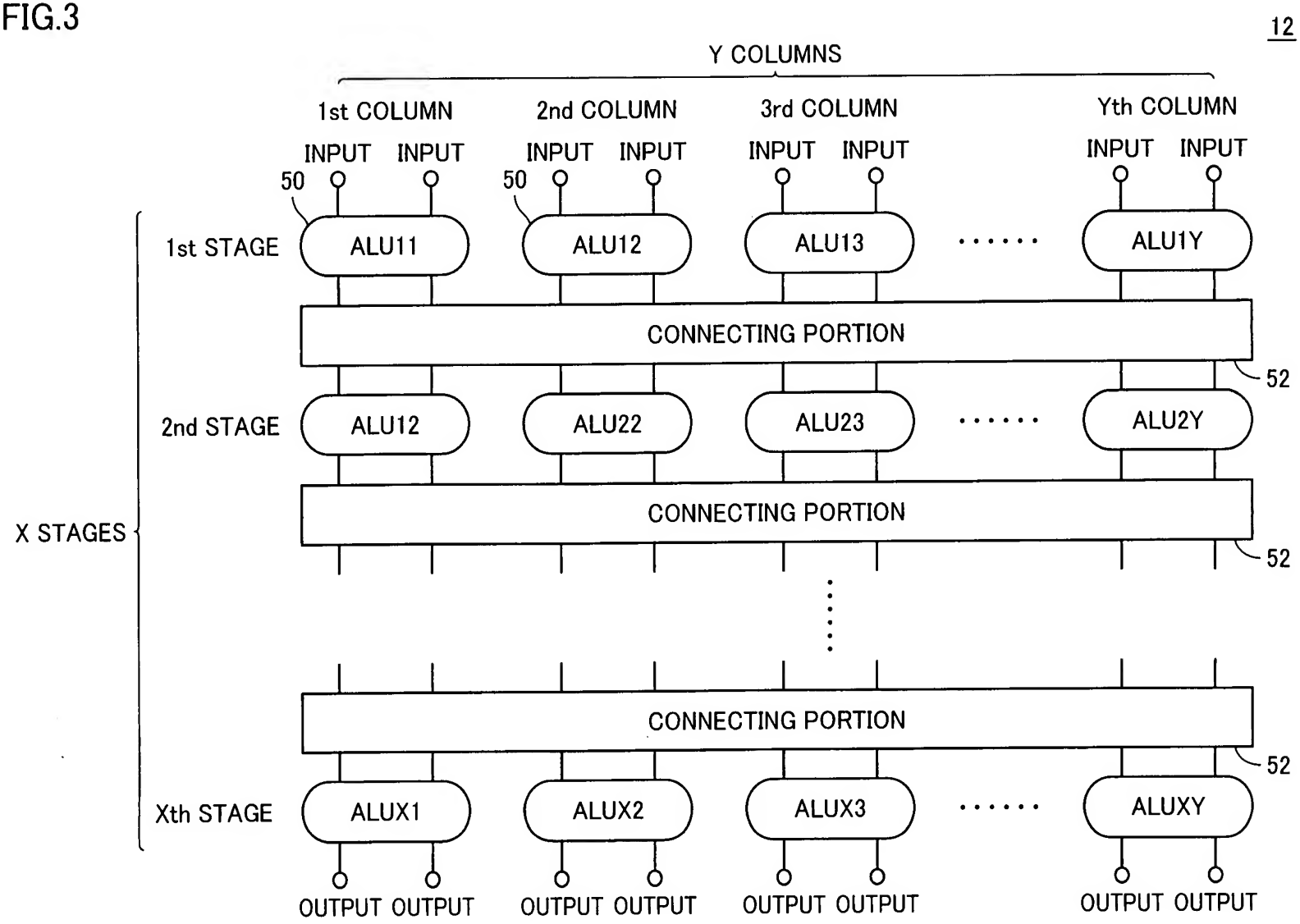

12
Y COLUMNS
1st COLUMN
2nd COLUMN
3rd COLUMN
Yth COLUMN
INPUT INPUT
50
1st STAGE
ALU11
ALU12
ALU13
ALU1Y
CONNECTING PORTION
52
2nd STAGE
ALU12
ALU22
ALU23
ALU2Y
X STAGES
Xth STAGE
ALUX1
ALUX2
ALUX3
ALUXY
OUTPUT OUTPUT

FIG.4

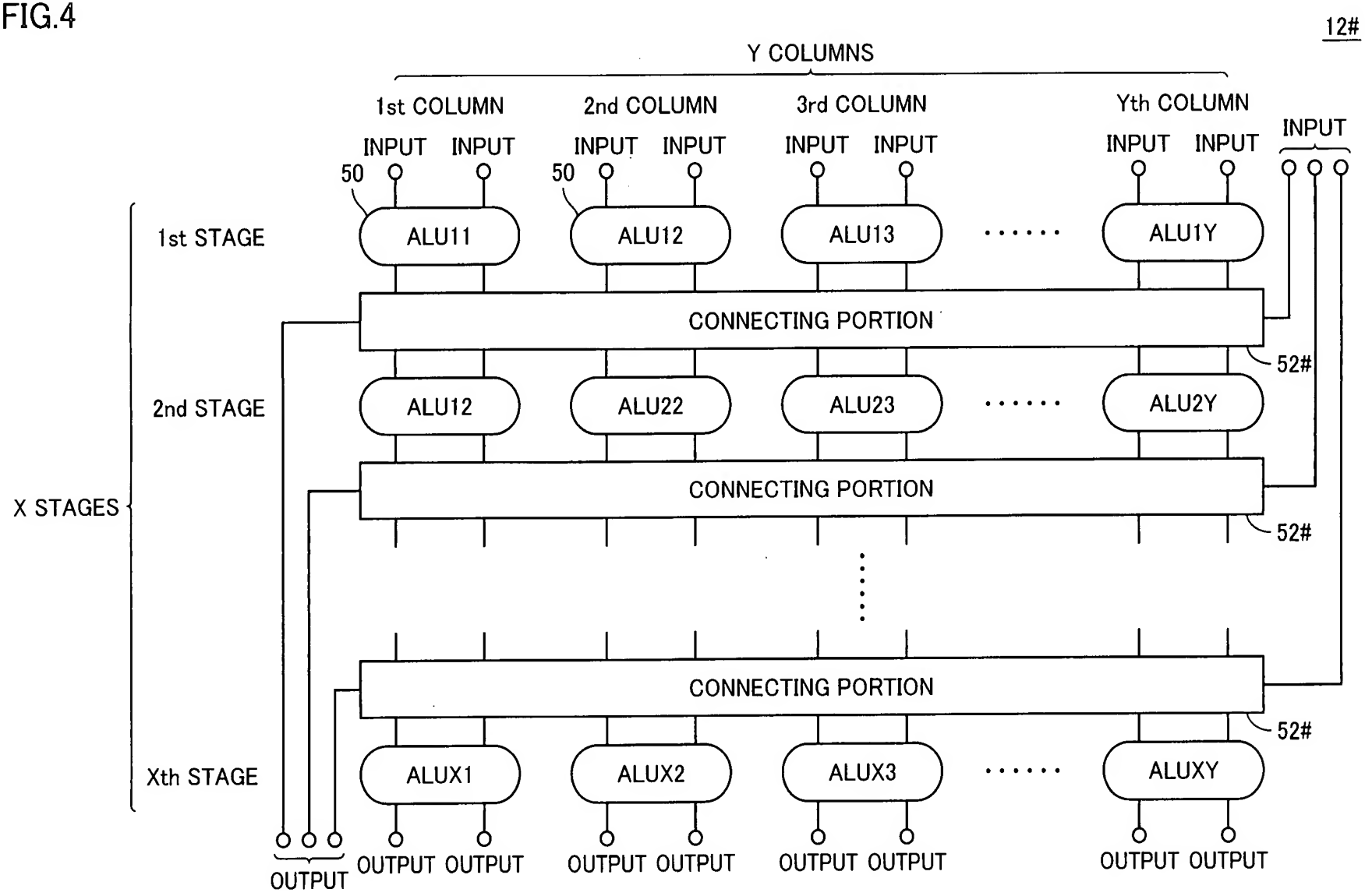

12#
Y COLUMNS
1st COLUMN
2nd COLUMN
3rd COLUMN
Yth COLUMN
INPUT
50
1st STAGE
2nd STAGE
Xth STAGE
X STAGES
ALU11
ALU12
ALU13
ALU1Y
CONNECTING PORTION
52#
ALU22
ALU23
ALU2Y
ALUX1
ALUX2
ALUX3
ALUXY
OUTPUT

FIG.5

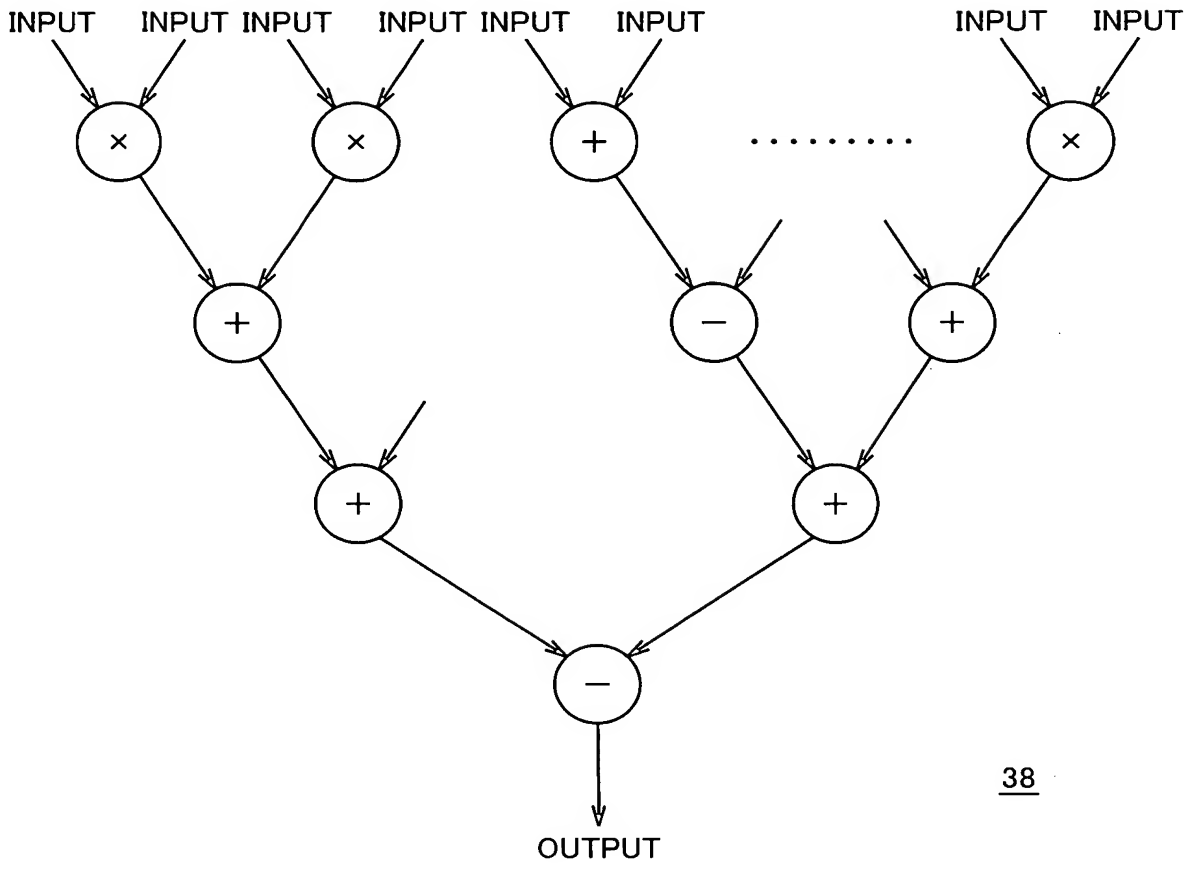


FIG.6

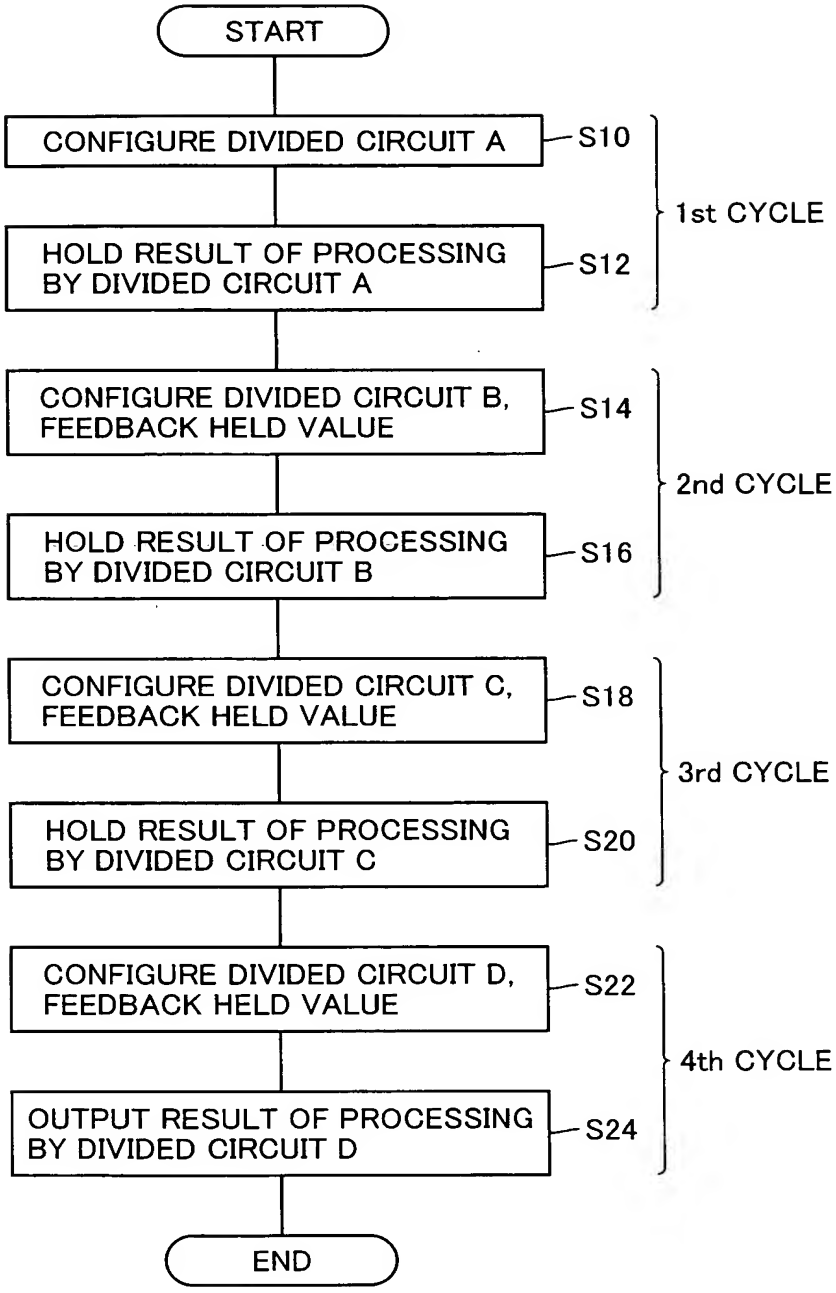

START
CONFIGURE DIVIDED CIRCUIT A
S10
HOLD RESULT OF PROCESSING BY DIVIDED CIRCUIT A
S12
1st CYCLE
CONFIGURE DIVIDED CIRCUIT B, FEEDBACK HELD VALUE
S14
HOLD RESULT OF PROCESSING BY DIVIDED CIRCUIT B
S16
2nd CYCLE
CONFIGURE DIVIDED CIRCUIT C, FEEDBACK HELD VALUE
S18
HOLD RESULT OF PROCESSING BY DIVIDED CIRCUIT C
S20
3rd CYCLE
CONFIGURE DIVIDED CIRCUIT D, FEEDBACK HELD VALUE
S22
OUTPUT RESULT OF PROCESSING BY DIVIDED CIRCUIT D
S24
4th CYCLE
END

FIG.7

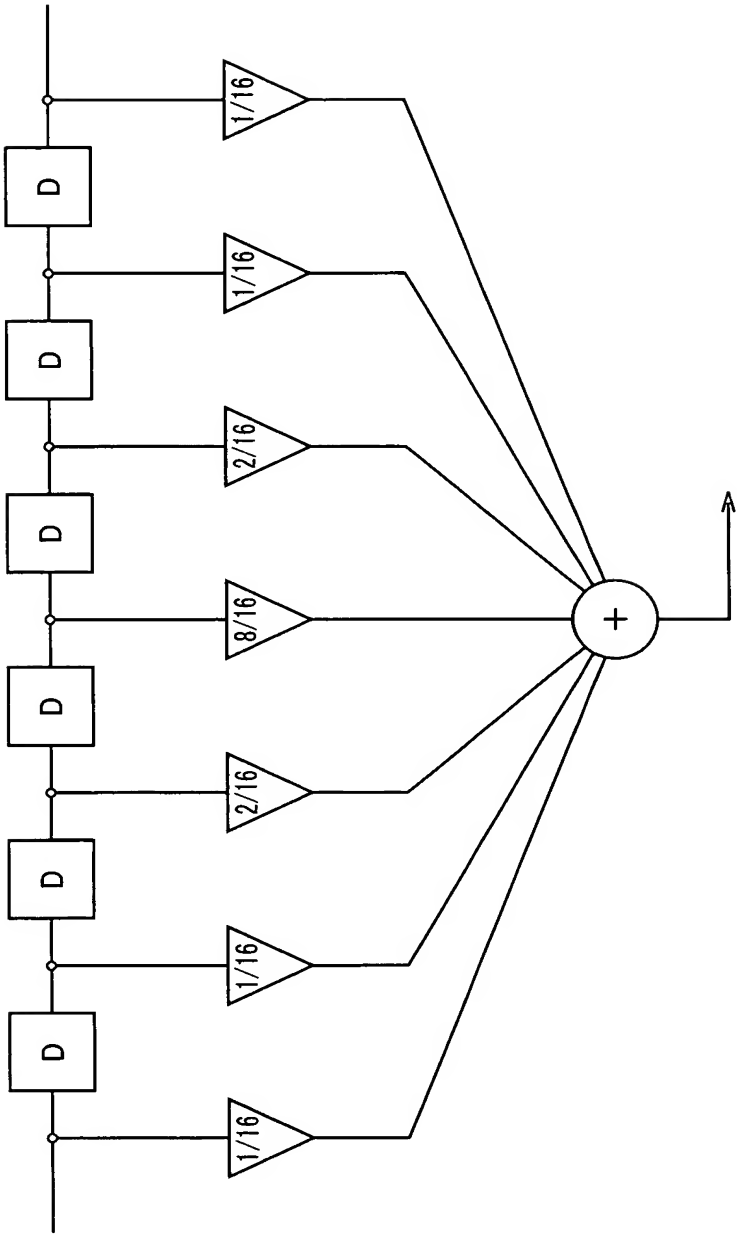


FIG.8

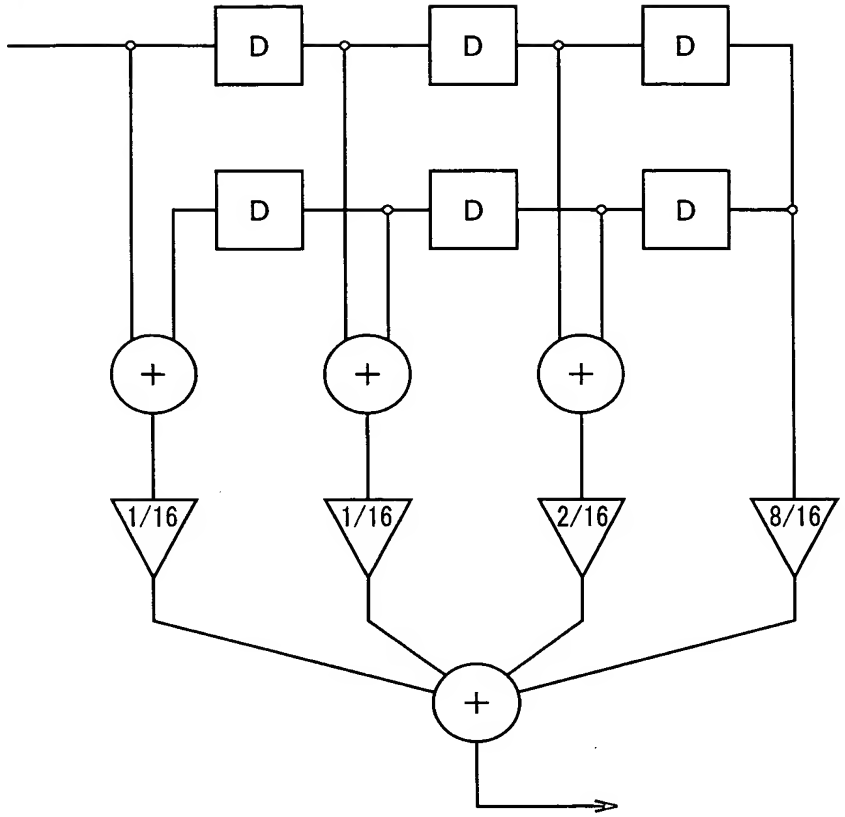


FIG.9

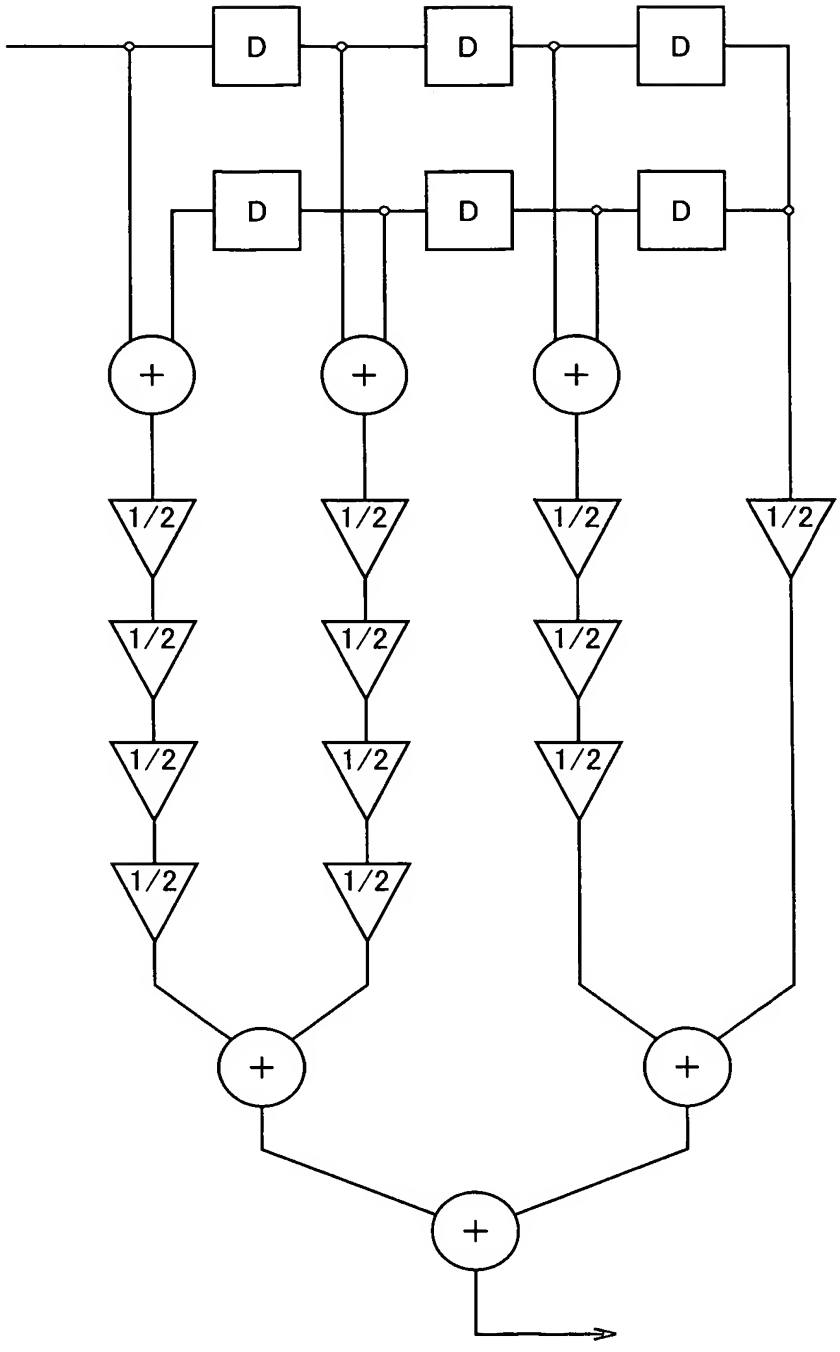
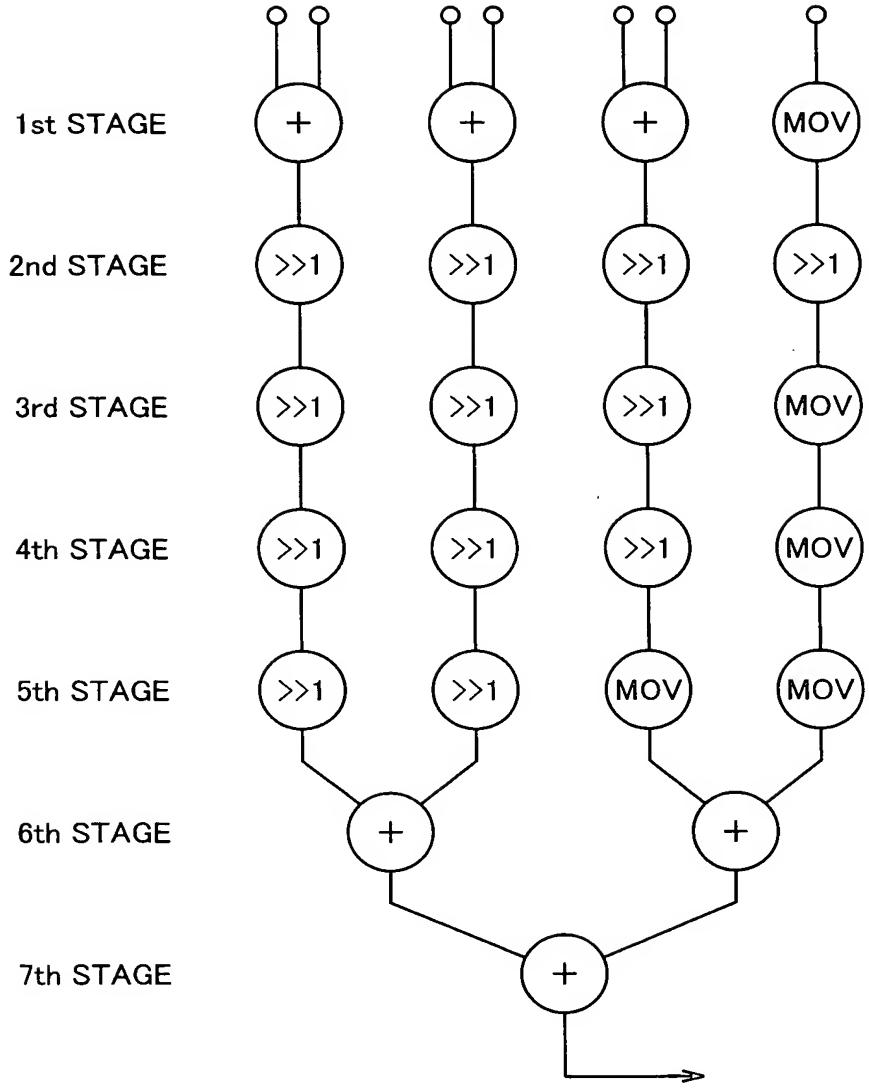


FIG.10


1st STAGE
2nd STAGE
3rd STAGE
4th STAGE
5th STAGE
6th STAGE
7th STAGE
+
MOV
>>1

38a

FIG.11

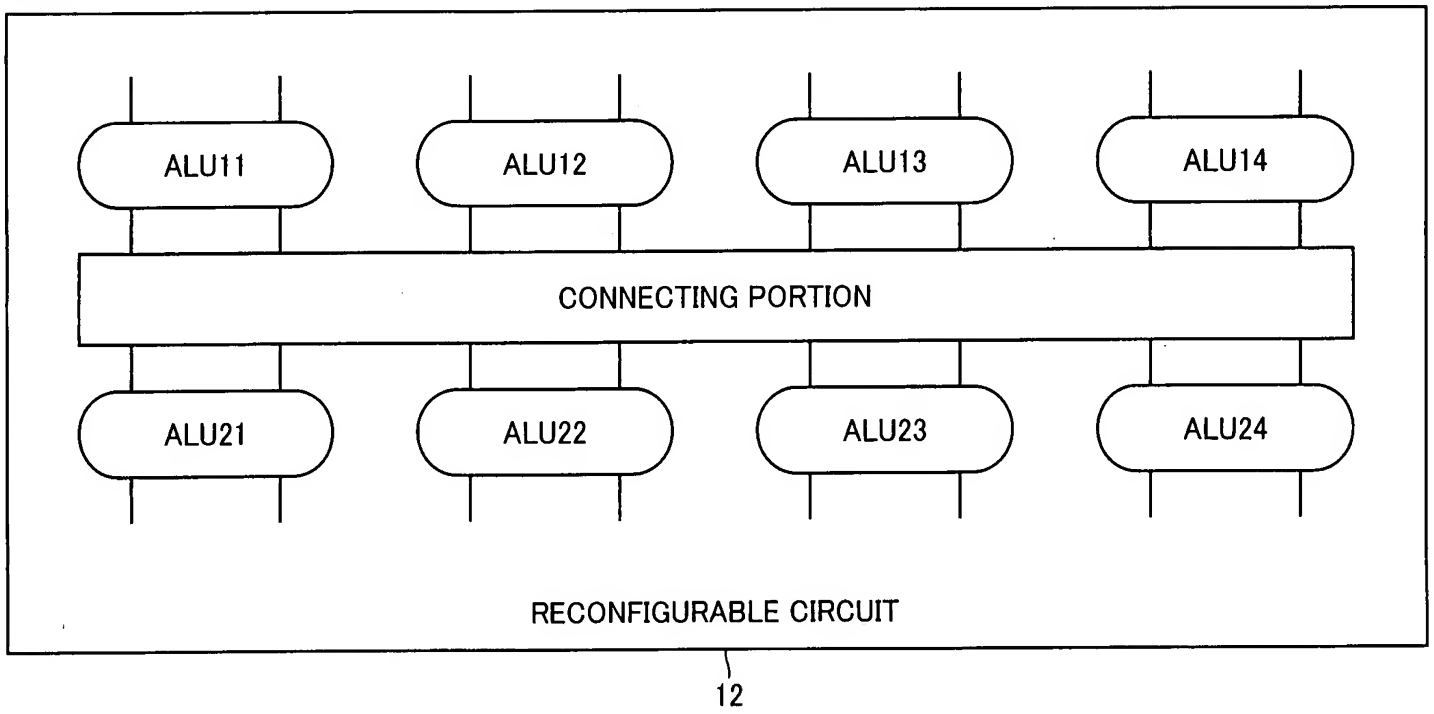

ALU11
ALU12
ALU13
ALU14
CONNECTING PORTION
ALU21
ALU22
ALU23
ALU24
RECONFIGURABLE CIRCUIT
12

FIG.12

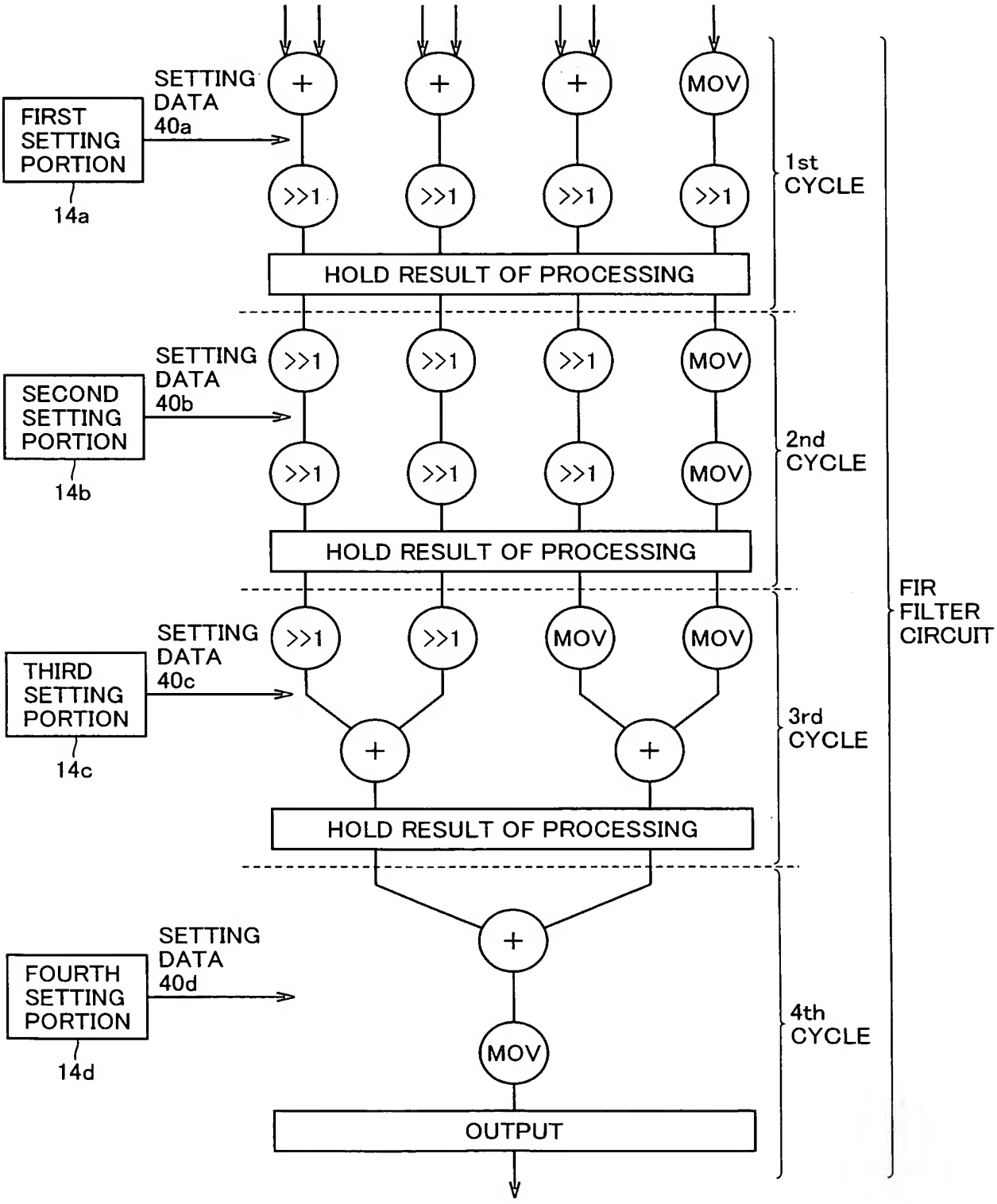

FIRST SETTING PORTION
14a
SETTING DATA 40a
SECOND SETTING PORTION
14b
SETTING DATA 40b
THIRD SETTING PORTION
14c
SETTING DATA 40c
FOURTH SETTING PORTION
14d
SETTING DATA 40d
+
>>1
MOV
HOLD RESULT OF PROCESSING
OUTPUT
1st CYCLE
2nd CYCLE
3rd CYCLE
4th CYCLE
FIR FILTER CIRCUIT

FIG.13

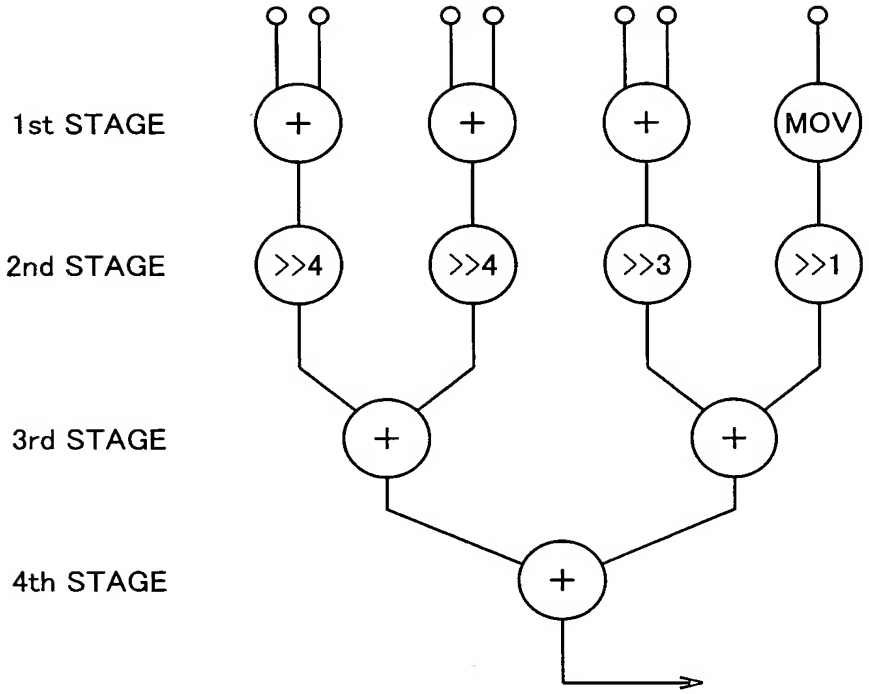


FIG.14

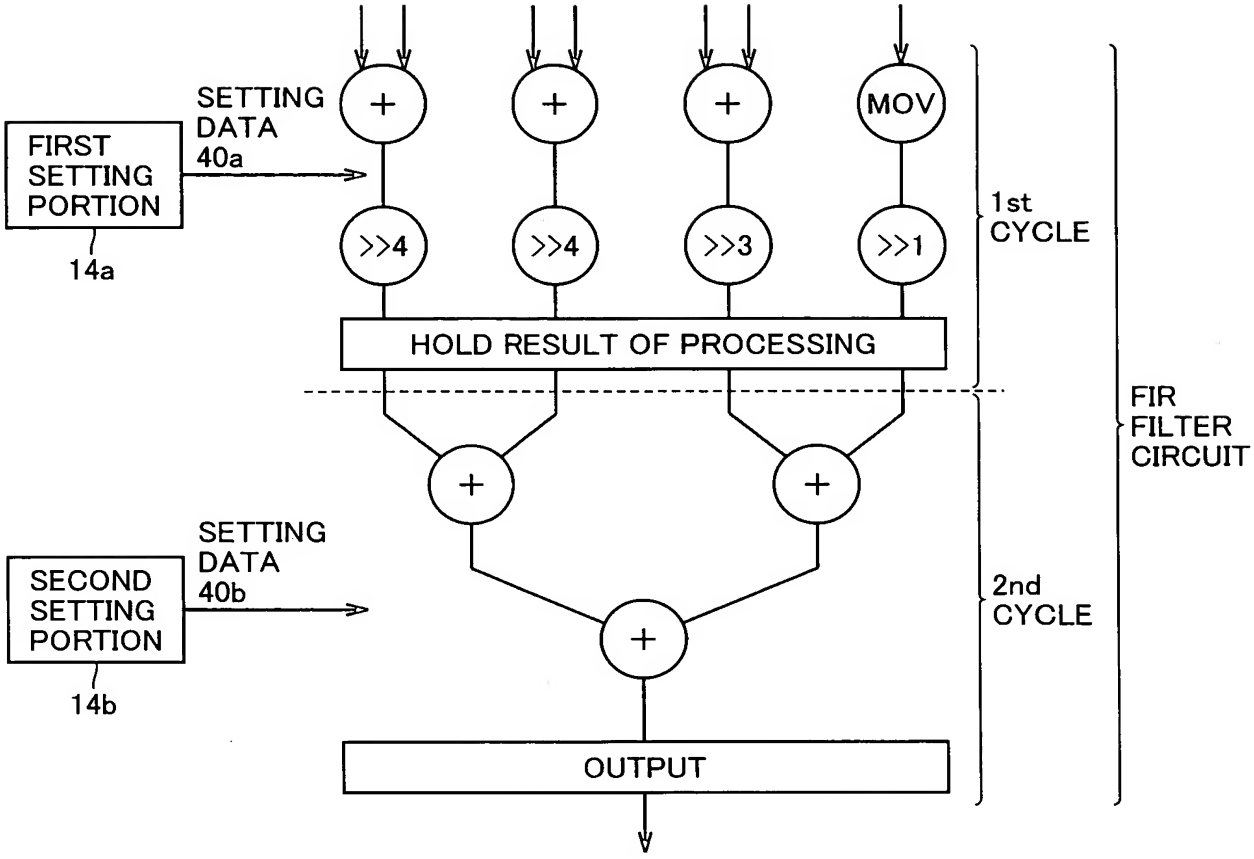

SETTING DATA 40a
FIRST SETTING PORTION
14a
+
+
+
MOV
>>4
>>4
>>3
>>1
1st CYCLE
HOLD RESULT OF PROCESSING
+
+
SETTING DATA 40b
SECOND SETTING PORTION
14b
+
2nd CYCLE
OUTPUT
FIR FILTER CIRCUIT

FIG.15

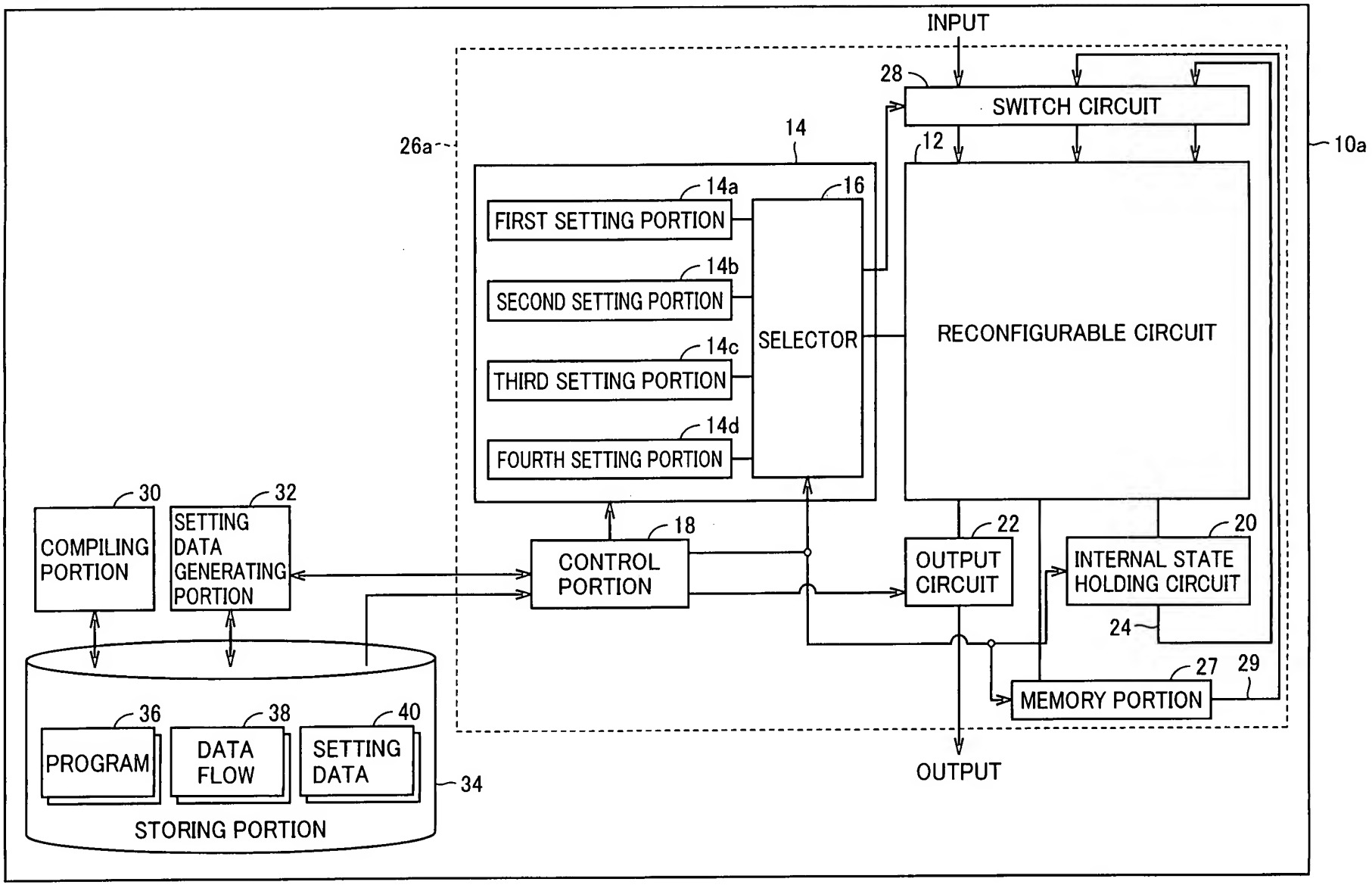

INPUT
28
SWITCH CIRCUIT
26a
14
12
10a
14a
16
FIRST SETTING PORTION
14b
SECOND SETTING PORTION
SELECTOR
RECONFIGURABLE CIRCUIT
14c
THIRD SETTING PORTION
14d
FOURTH SETTING PORTION
30
32
COMPILING PORTION
SETTING DATA GENERATING PORTION
18
CONTROL PORTION
22
OUTPUT CIRCUIT
20
INTERNAL STATE HOLDING CIRCUIT
24
27
29
MEMORY PORTION
36
38
40
PROGRAM
DATA FLOW
SETTING DATA
34
STORING PORTION
OUTPUT

FIG.16

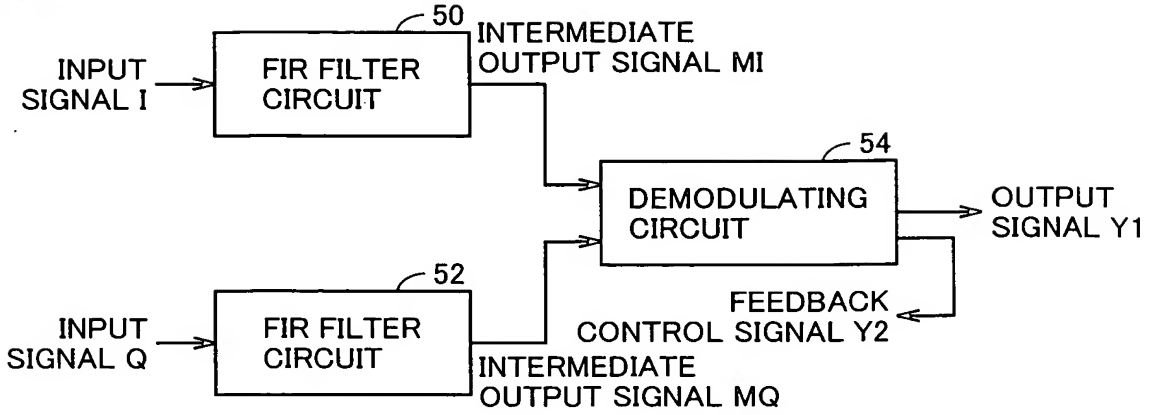

50
INPUT SIGNAL I
FIR FILTER CIRCUIT
INTERMEDIATE OUTPUT SIGNAL MI
54
DEMODULATING CIRCUIT
OUTPUT SIGNAL Y1
FEEDBACK CONTROL SIGNAL Y2
52
INPUT SIGNAL Q
FIR FILTER CIRCUIT
INTERMEDIATE OUTPUT SIGNAL MQ

FIG.17

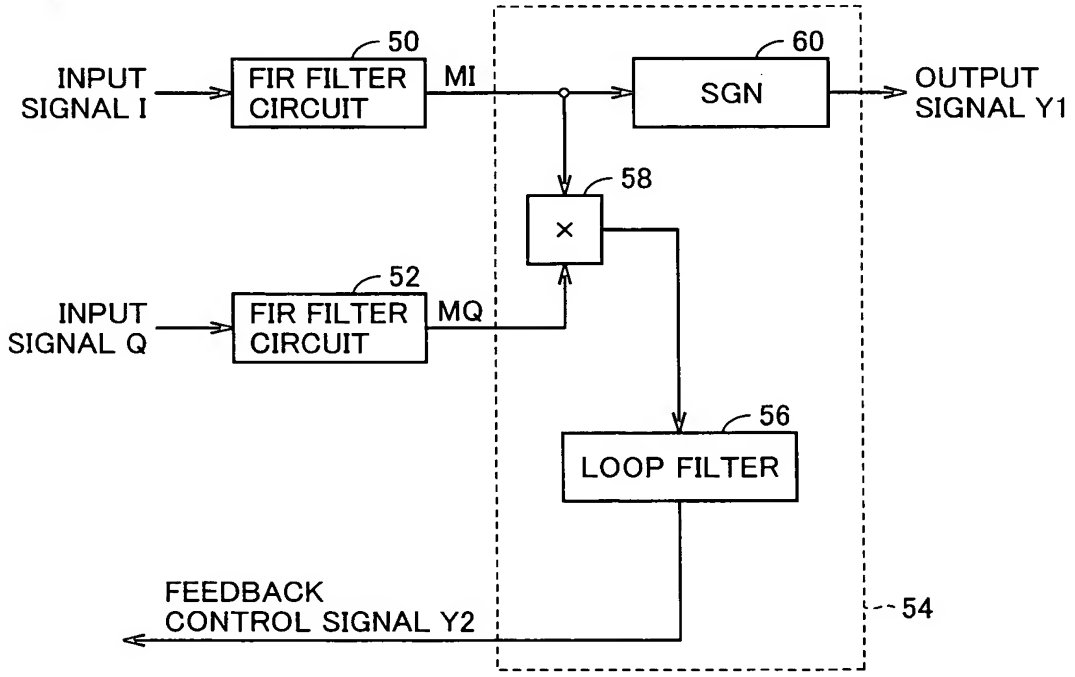

50
INPUT SIGNAL I
FIR FILTER CIRCUIT
MI
60
SGN
OUTPUT SIGNAL Y1
58
×
52
INPUT SIGNAL Q
FIR FILTER CIRCUIT
MQ
56
LOOP FILTER
FEEDBACK CONTROL SIGNAL Y2
54

FIG.18

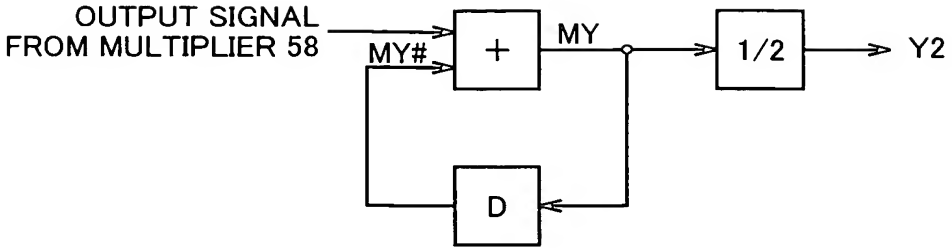
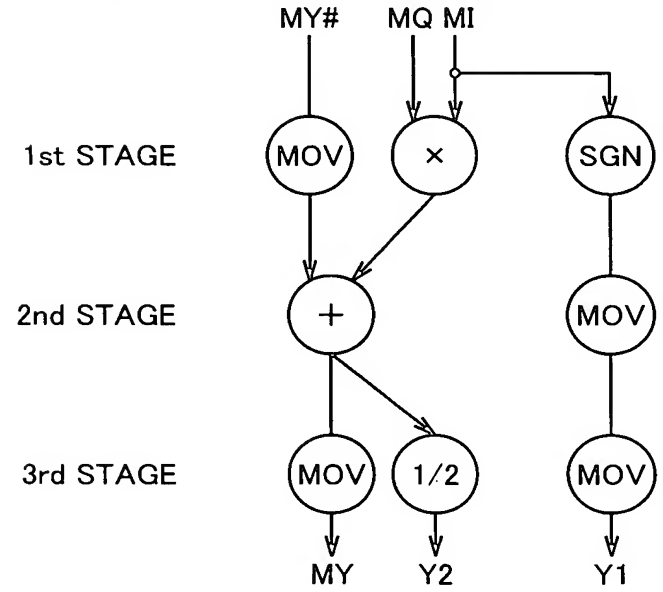


FIG.19



38c

FIG.20

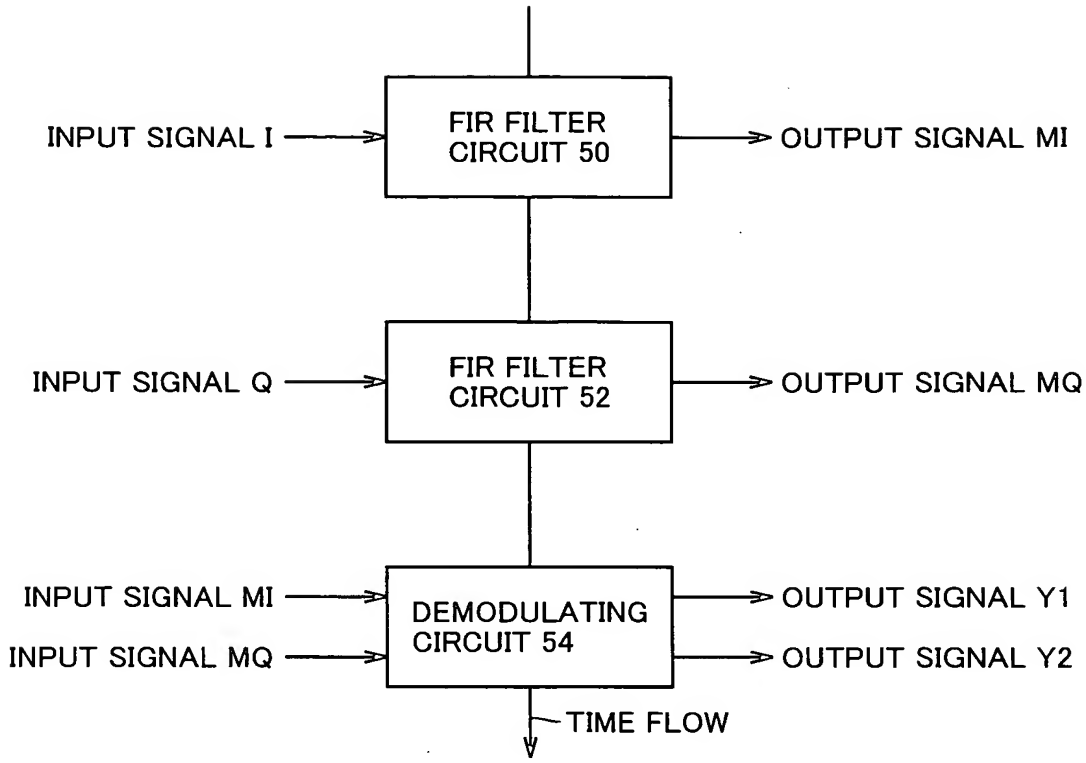

INPUT SIGNAL I
FIR FILTER CIRCUIT 50
OUTPUT SIGNAL MI
INPUT SIGNAL Q
FIR FILTER CIRCUIT 52
OUTPUT SIGNAL MQ
INPUT SIGNAL MI
INPUT SIGNAL MQ
DEMODULATING CIRCUIT 54
OUTPUT SIGNAL Y1
OUTPUT SIGNAL Y2
TIME FLOW

FIG.21

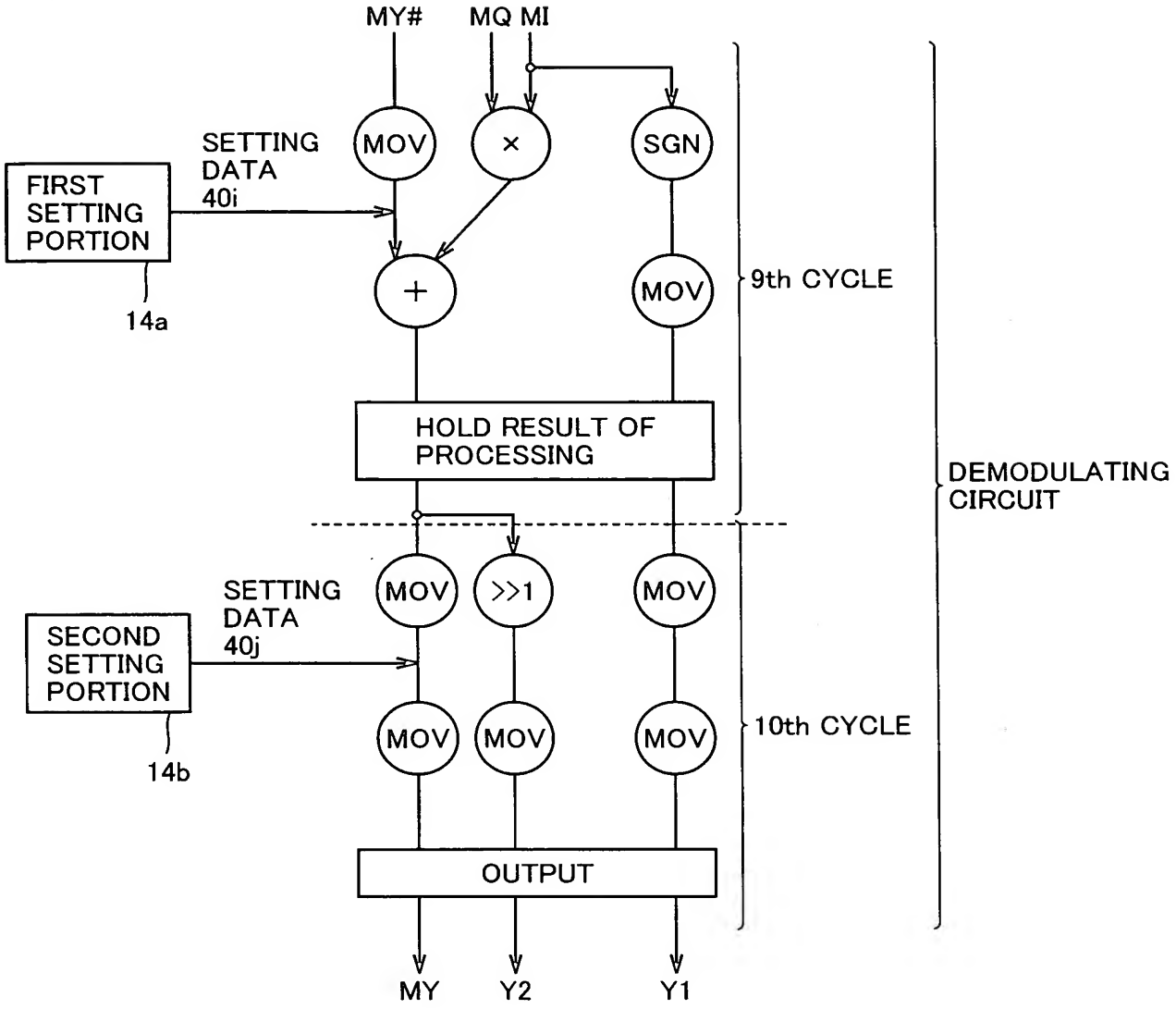

MY#
MQ MI
SETTING DATA 40i
MOV
×
SGN
FIRST SETTING PORTION
14a
+
MOV
9th CYCLE
HOLD RESULT OF PROCESSING
DEMODULATING CIRCUIT
SETTING DATA 40j
MOV
>>1
MOV
SECOND SETTING PORTION
14b
MOV
MOV
MOV
10th CYCLE
OUTPUT
MY
Y2
Y1

FIG.22

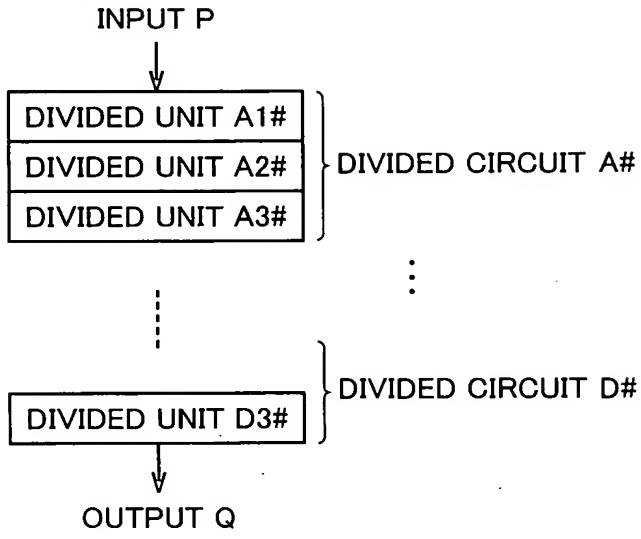


FIG.23

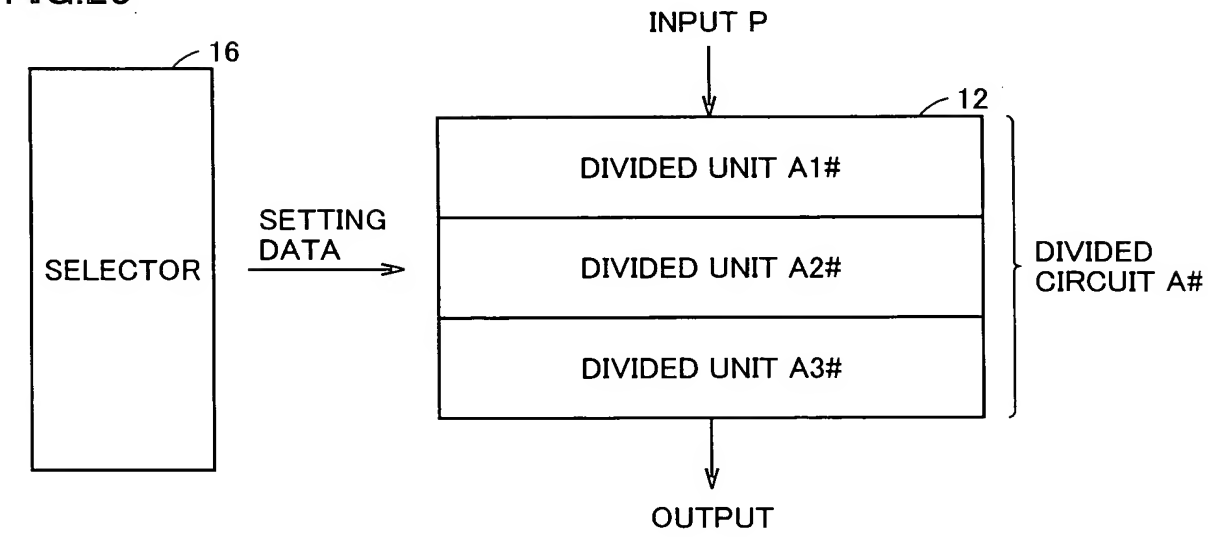


FIG.24

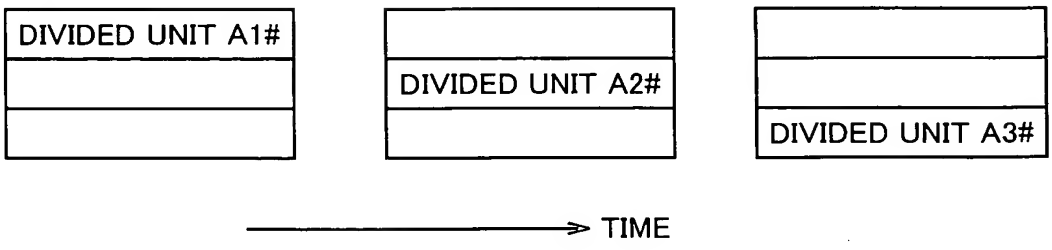


FIG.25

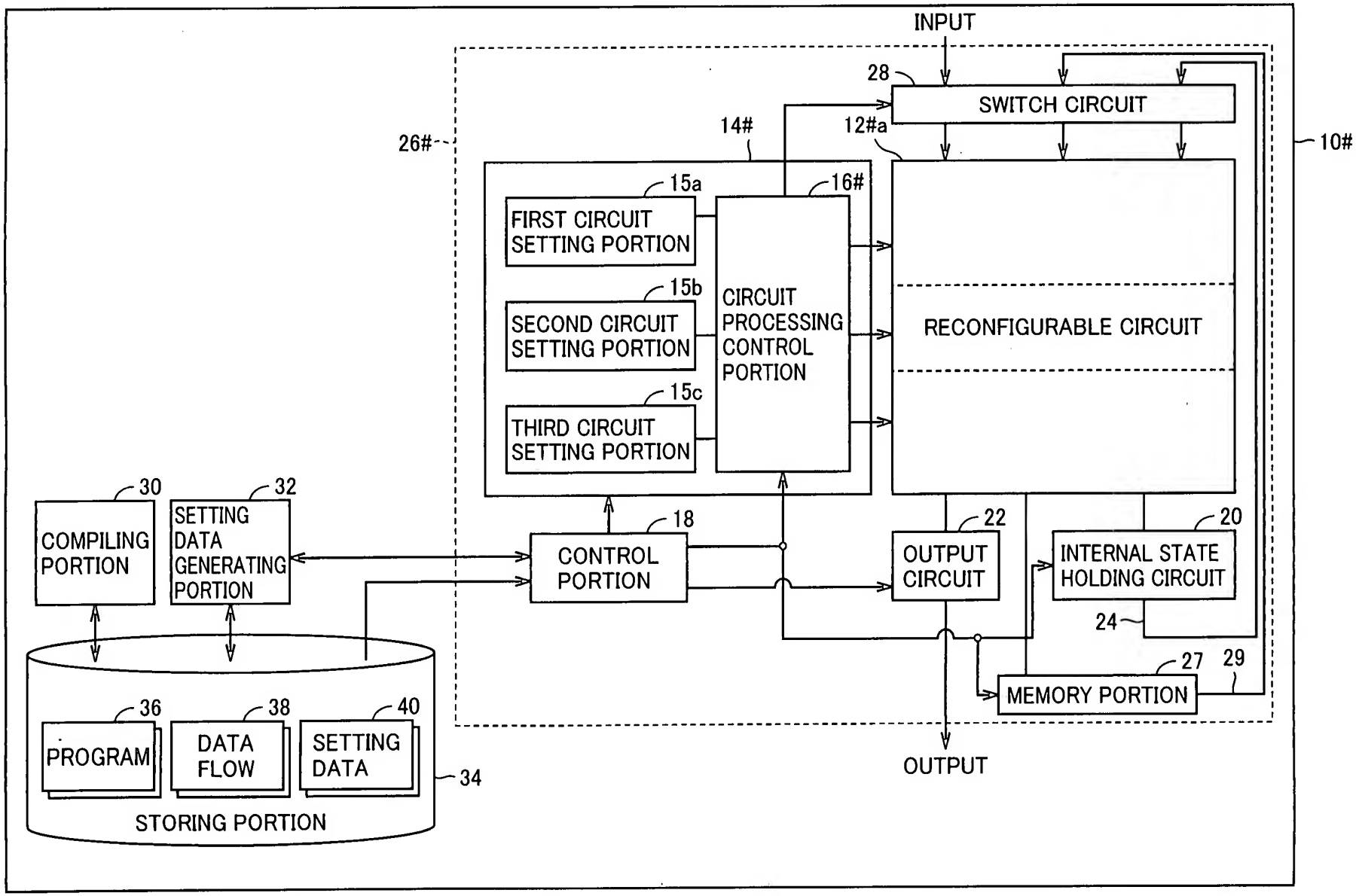

INPUT
28
SWITCH CIRCUIT
26#
14#
12#a
10#
15a
16#
FIRST CIRCUIT SETTING PORTION
15b
SECOND CIRCUIT SETTING PORTION
15c
THIRD CIRCUIT SETTING PORTION
CIRCUIT PROCESSING CONTROL PORTION
RECONFIGURABLE CIRCUIT
30
COMPILING PORTION
32
SETTING DATA GENERATING PORTION
18
CONTROL PORTION
22
OUTPUT CIRCUIT
20
INTERNAL STATE HOLDING CIRCUIT
24
27
29
MEMORY PORTION
OUTPUT
36
PROGRAM
38
DATA FLOW
40
SETTING DATA
34
STORING PORTION

FIG.26

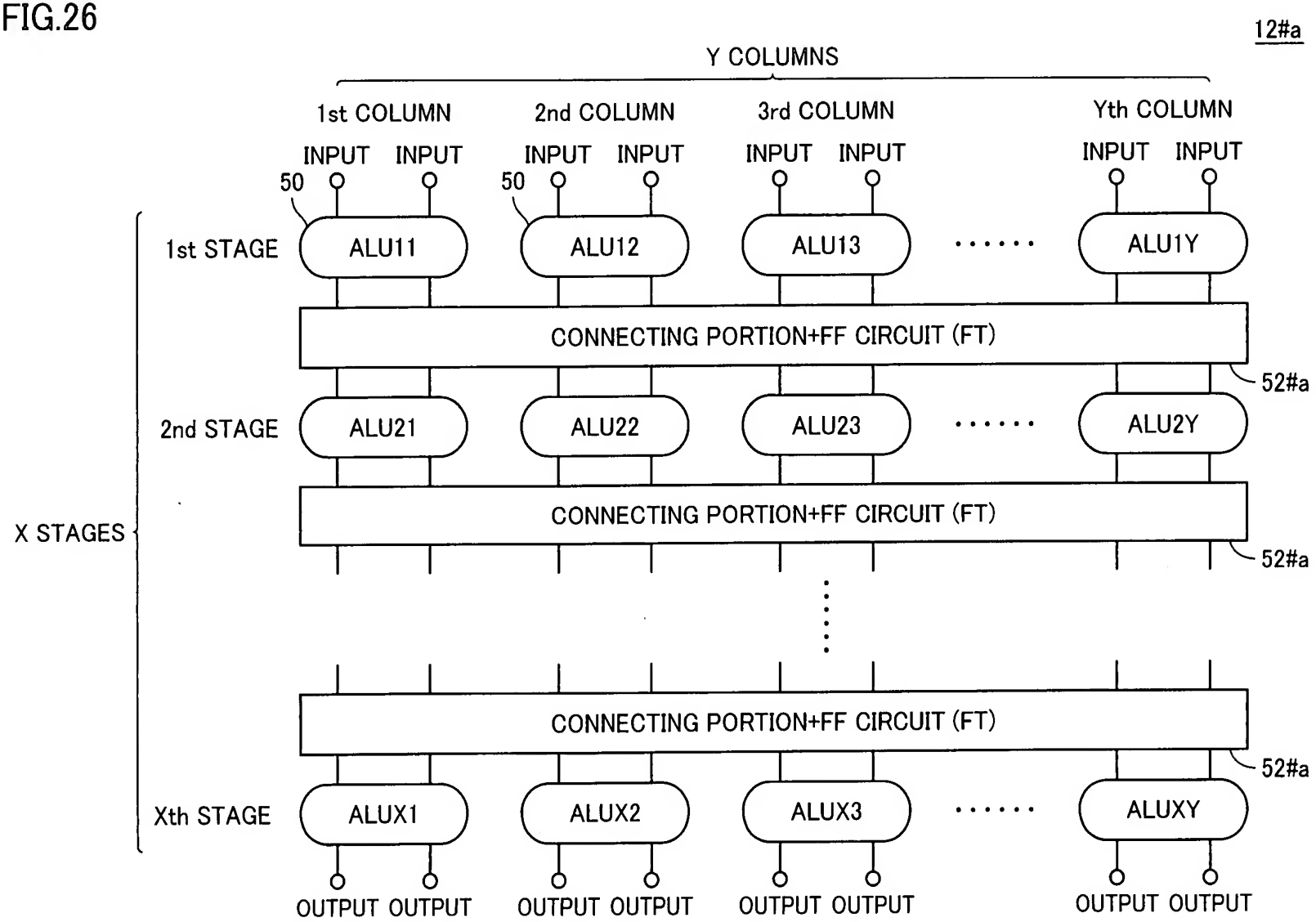

12#a
Y COLUMNS
1st COLUMN
2nd COLUMN
3rd COLUMN
Yth COLUMN
INPUT INPUT
50
1st STAGE
ALU11
ALU12
ALU13
ALU1Y
CONNECTING PORTION+FF CIRCUIT (FT)
52#a
2nd STAGE
ALU21
ALU22
ALU23
ALU2Y
X STAGES
Xth STAGE
ALUX1
ALUX2
ALUX3
ALUXY
OUTPUT OUTPUT

FIG.27

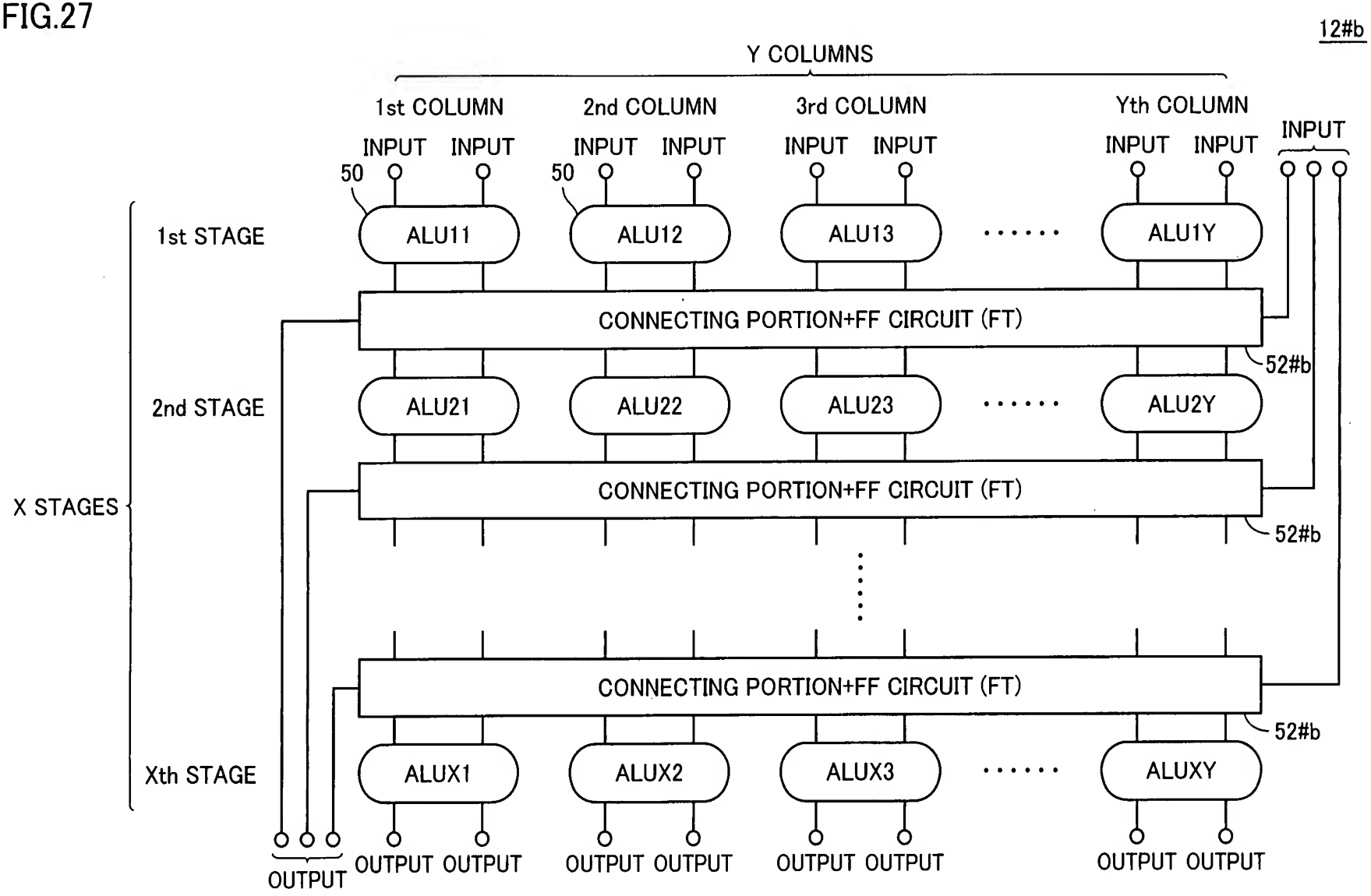

12#b
Y COLUMNS
1st COLUMN
2nd COLUMN
3rd COLUMN
Yth COLUMN
INPUT
50
ALU11
ALU12
ALU13
ALU1Y
1st STAGE
CONNECTING PORTION+FF CIRCUIT (FT)
52#b
ALU21
ALU22
ALU23
ALU2Y
2nd STAGE
X STAGES
ALUX1
ALUX2
ALUX3
ALUXY
Xth STAGE
OUTPUT

FIG.28

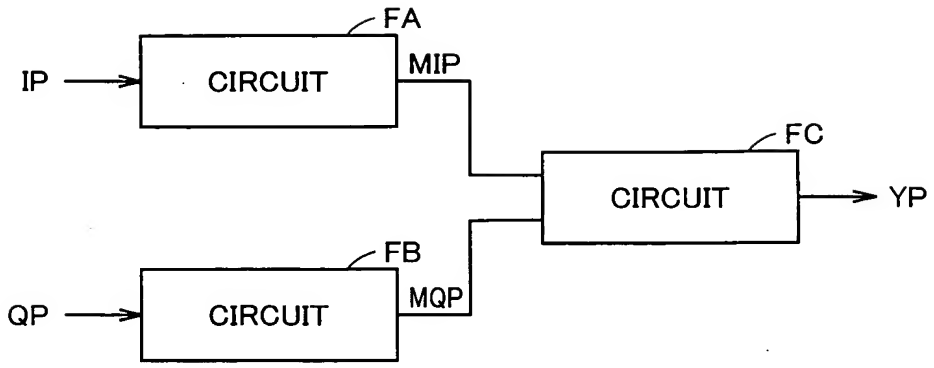


FIG.29A

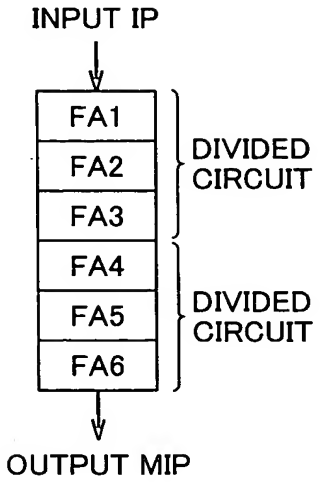


FIG.29B

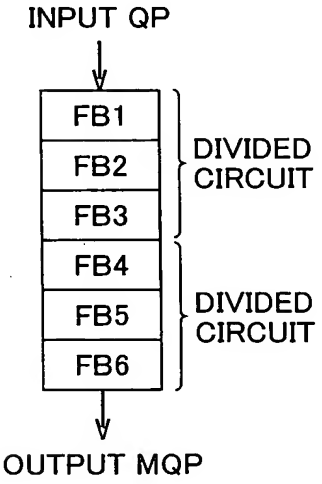


FIG.29C

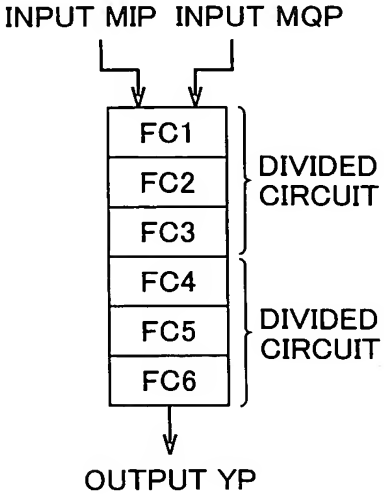


FIG.30

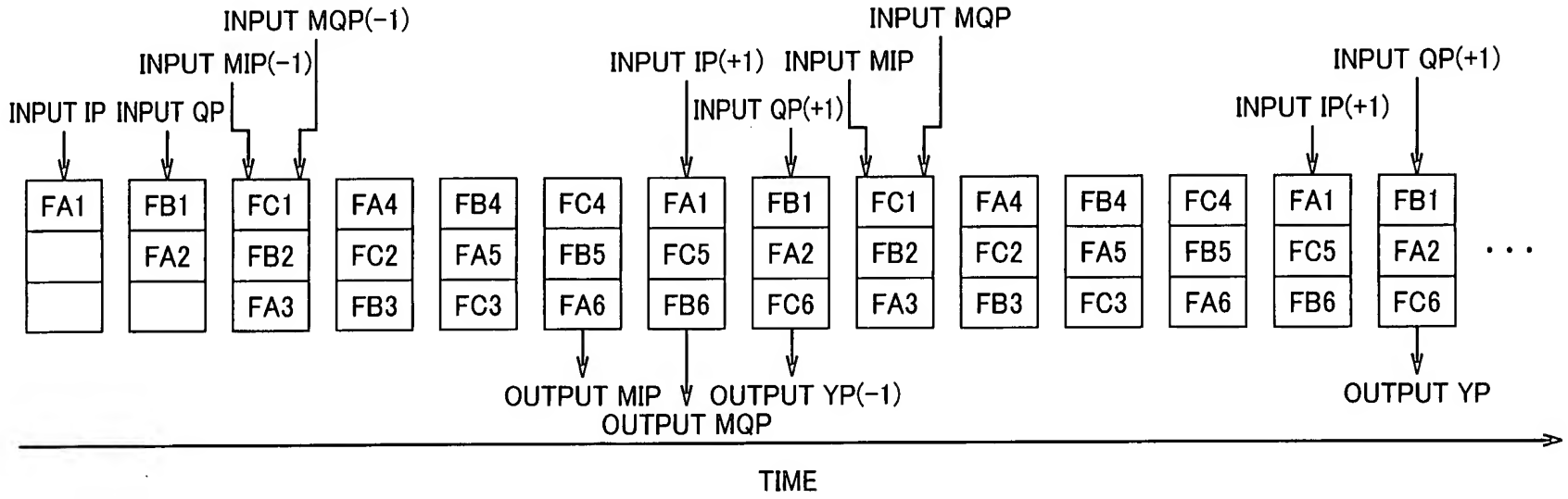

INPUT MQP(-1)
INPUT MIP(-1)
INPUT IP
INPUT QP
INPUT IP(+1)
INPUT MIP
INPUT MQP
INPUT QP(+1)
INPUT QP(+1)
INPUT IP(+1)
FA1
FB1
FC1
FA4
FB4
FC4
FA1
FB1
FC1
FA4
FB4
FC4
FA1
FB1
FA2
FB2
FC2
FA5
FB5
FC5
FA2
FB2
FC2
FA5
FB5
FC5
FA2
FA3
FB3
FC3
FA6
FB6
FC6
FA3
FB3
FC3
FA6
FB6
FC6
OUTPUT MIP
OUTPUT YP(-1)
OUTPUT MQP
OUTPUT YP
TIME

FIG.31

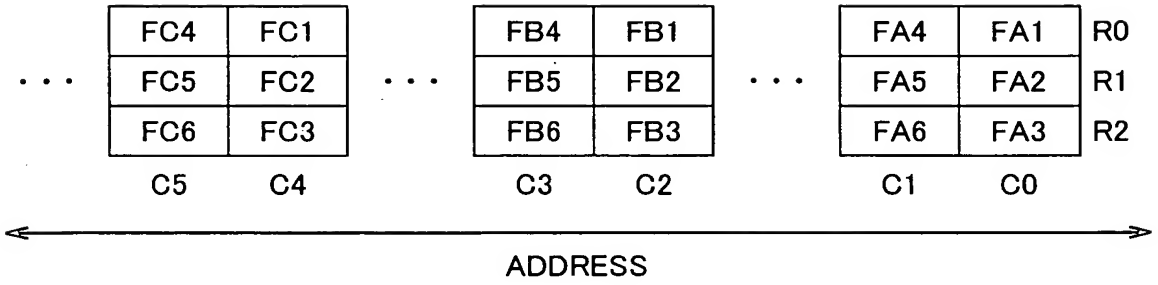


FIG.32

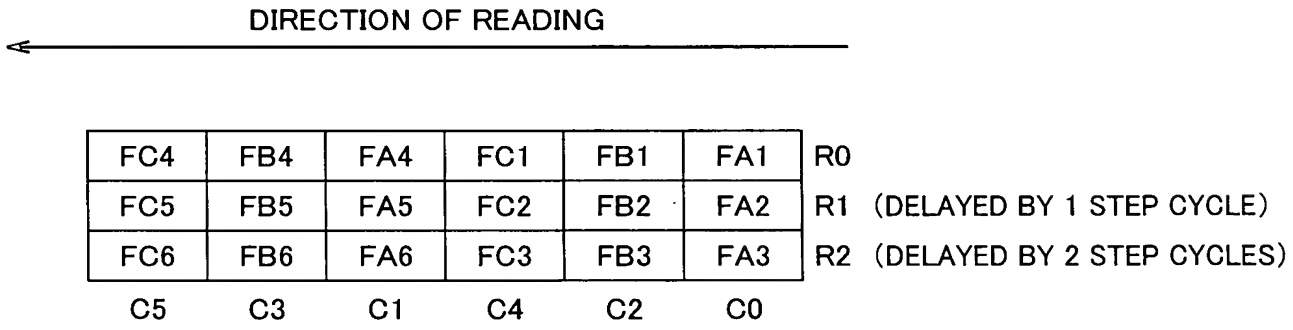


FIG.33

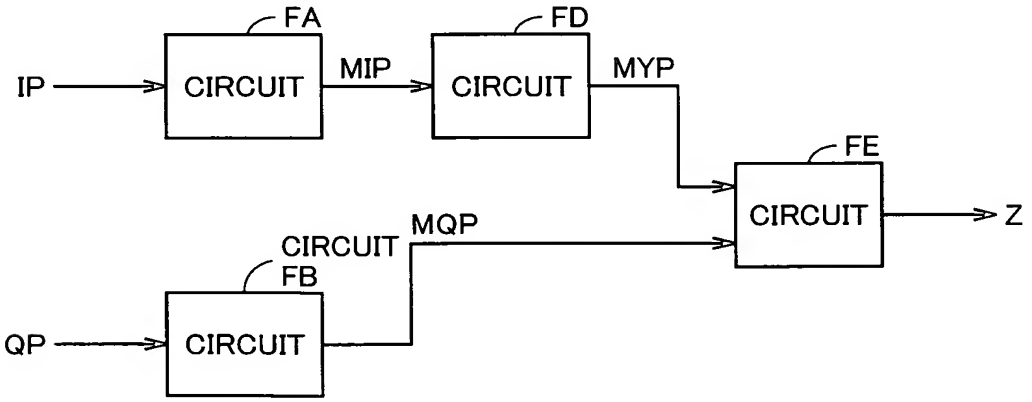


FIG.34A

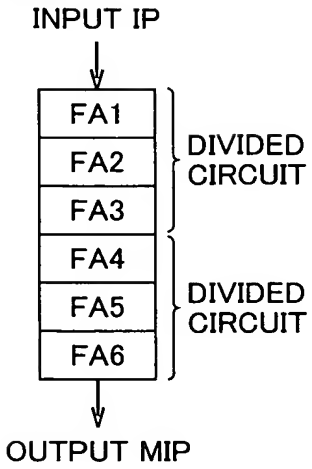


FIG.34B

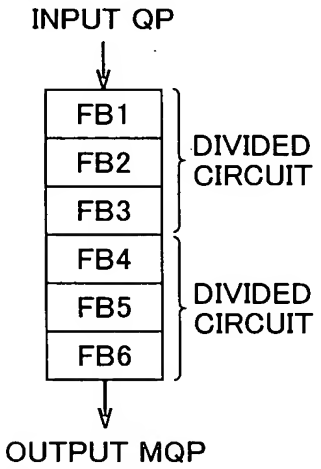


FIG.34C

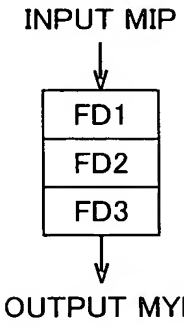


FIG.34D

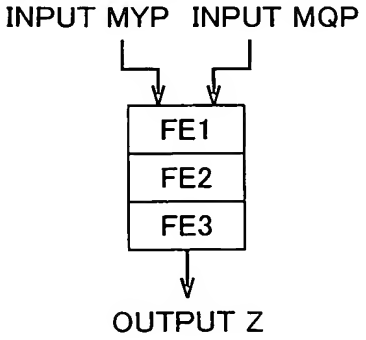


FIG.35

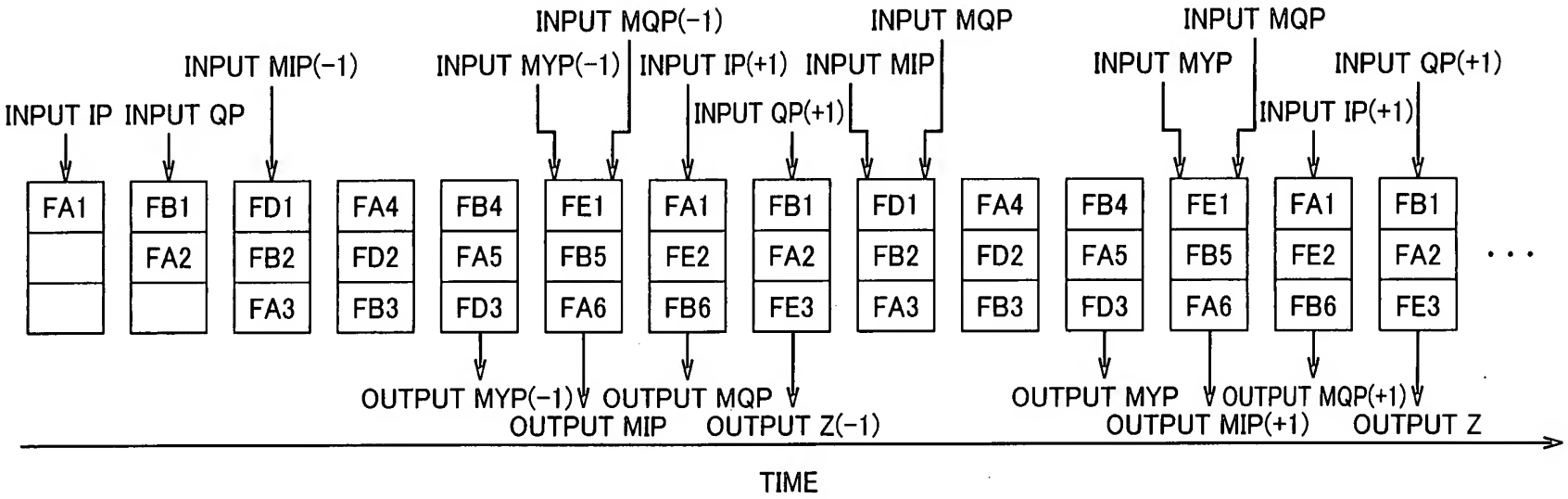

INPUT IP
INPUT QP
INPUT MIP(-1)
INPUT MYP(-1)
INPUT MQP(-1)
INPUT IP(+1)
INPUT QP(+1)
INPUT MIP
INPUT MQP
INPUT MYP
INPUT IP(+1)
INPUT QP(+1)
INPUT MQP
FA1 FB1 FD1 FA4 FB4 FE1 FA1 FB1 FD1 FA4 FB4 FE1 FA1 FB1
FA2 FB2 FD2 FA5 FB5 FE2 FA2 FB2 FD2 FA5 FB5 FE2 FA2
FA3 FB3 FD3 FA6 FB6 FE3 FA3 FB3 FD3 FA6 FB6 FE3
OUTPUT MYP(-1)
OUTPUT MIP
OUTPUT MQP
OUTPUT Z(-1)
OUTPUT MYP
OUTPUT MIP(+1)
OUTPUT MQP(+1)
OUTPUT Z
TIME

FIG.36A

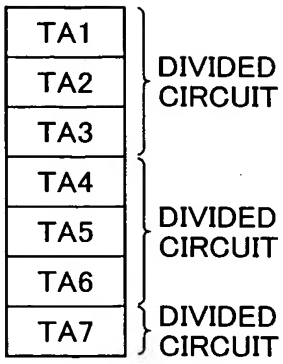


FIG.36B

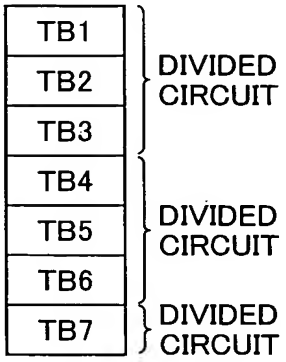


FIG.36C

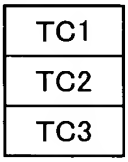


FIG.37